聯陽半導體
ITE Tech. Inc.

IT9852E
IT9854E
IT9856TE

HD Display and Smart Control SoC

Preliminary Specification V0.9

ITE TECH. INC.

1. Features

■ **Host Processor**
- 400MHz 32-bit ARM9 CPU
- 16KB instruction cache and 16KB data cache

■ **Audio Processor**
- 200MHz 32-bit RISC CPU with DSP extensions
- 8KB instruction cache, 8KB data cache
- Supports audio CODEC
  - MPEG 1/2/2.5 audio layer 1/2/3
  - WMA decoder
  - MPEG-2/4 AAC-LC decoder
  - FLAC decoder

■ **Micro Controller**
- 200MHz 32-bit RISC CPU
- 16KB SRAM for instruction/data access

■ **Display Interface**
- 1280x800 16/18/24 bpp (RGB565/RGB666/RGB8888)
- Resolution: Max. 4096*4096 true color mode
- Supports 6/9/16/18/24 bits RGB I/F and 8/9/16/18/24 bits CPU I/F
- Supports C-STN with frame buffer
- HW 90°/180°/270° rotate and mirror
- Supports TFT or TFD (with or without frame-buffer)
- Supports three channel gamma correction
- Supports hardware cursor
- Supports CCIR601/CCIR656 interface
- Supports digital TCON

■ **2D Graphics Acceleration**
- Bit Block Transfer (BitBlt) with ROP3 operation
- Supports mask plan with 1bpp, 2bpp, 4bpp and 8bpp format.
- Supports color expansion with 1bpp, 2bpp, 4bpp and 8bpp format
- Coordinates transform
- One clipping window

■ **USB Host/Device**
- Provides two host/device controller
- Compliant with USB specification version 2.0
- Compatible with EHCI 1.0
- Supports point-to-point communications with one HS/FS/LS device
- Both host and device support isochronous/interrupt/control/bulk transfers
- Compatible with EHCI data structures

■ **Memory Controller**
- Supports maximum 256MByte 16-bit DDR/DDR2
- Supports Ping-Pong bank with tilling memory access

■ **Ethernet MAC**
- Compliant with full IEEE 802.3-2002 specifications
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Supports CSMA/CD Protocol for Half-Duplex operation
- Supports IEEE 802.3x flow-control for Full-Duplex operation
- Supports IEEE 1588-2002 Time stamping on the transmit and received frames
- IEEE 802.3 compliant RMII PHY interface

■ **JPEG Encoder/Decoder**
- Fully compliant with Baseline JPEG standard ISO/IEC 10918
- Supports up to 256 million pixel (16376 * 16376)
- Supports 422, 420, 411, 400, 444 decode
- Supports 422, 420 encode
- Supports downloadable Quantization and Huffman table
- Interleaved and non-interleave scan decode
- Supports motion JPEG for 720p@30fps (1280x720)

■ **Video Encoder/Decoder**
- H.264 Decoder
  - High/main profile, level 3.1
  - B Frame not supported
  - Real-time decode for 720p@30fps (1280x720)

■ **Image Signal Processor**
- Input data YUV format: 444, 420, 422
- Output data RGB format: 888, 565, 444
- Image and video scaling engine for scaling up and down
- 2-tap vertical, 2-tap horizontal scaling filter
- Configurable filter coefficients
- Supports color correction matrix
- Supports color conversion
- Supports de-interlace filter
- Supports 2 layer High color OSD
- Supports dither for 4-, 5-, 6-bits RGB channel precision

■ **DMA**
- Provides 8 configurable DMA channels
- Supports chain transfer
- Memory-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfer
- Group round-robin arbitration scheme with 4 priority levels
- Supports 8-, 16-, and 32-bit wide data transaction
- Supports big-endian and little-endian

■ **Power Management**
- Flexible clock divider to slow down clock
- Dynamic gating clock
- Separate clock source to disable unused peripherals
- Wakeup from external event

■ **GPIO**
- Independent input, output and output enable buses for bi-directional I/O pins
- Each port can separately trigger the GPIO interrupt when it is programmed as input pin.
- Each port interrupt generation can be triggered by rising edge, falling edge, both edges, or high/low level when the interrupt option is set.

■ **IIC**
- Provides two IIC interfaces
- Supports standard, and fast mode through programming the clock division register
- Supports 7-bit, 10-bit and general call addressing mode
- Glitch suppression throughout the de-bounce circuit
- Programmable slave address
- Master-transmit, Master-receive, Slave-transmit and Slave-receive modes provided
- Configurable multi-master mode supported
- Slave mode general call address detection

■ **UART/IrDA**
- Four UART interfaces
- Baud rate up to 6.25M bps
- Firmware compatible with high-speed NS 16C550A UART
- IrDA 1.3 SIR with up to 115.2kbps data rate
- SIR pulse width programmable as 1.6us or 3/16 of the baud-rate pulse width
- Supports IrDA 1.3 FIR
- Multi-frame transmission and reception in FIR mode

■ **Interrupt Controller**
- Provides both edge and level-triggered interrupt sources with positive and negative directions
- Provides de-bounce circuit for interrupt source

■ **PWM**
- Provides six independent 32-bit timers with PWM
- Programmable duty cycle and frequency
- Supports external clock source
- It can merge two timers into a 64-bit timer.
- Supports incrementing and decrementing mode

■ **SPI**
- Supports TI SSP, Motorola SPI, National Semiconductor Microwire, and SPIDIF interface
- Supports master and slave modes
- Internally or externally controlled serial bit clock
- Internally or externally controlled frame/sync
- Programmable frame/sync polarity
- Programmable serial bit clock polarity, phase, and frequency
- Programmable serial bit data sequence (MSB or LSB first)
- Programmable threshold interrupt of transmit/receive FIFO

■ **RTC**
- Separated second, minute, hour, and day counter
- Programmable auto second, minute, hour or day alarm
- Generates power on signal when alarm occurs

■ **Remote Controller**
- Hardware programmable to receive remote controller signal

■ **Wiegand Controller**
- Provides two Wiegand interfaces
- Supports up to maximum 128-bit code length
- Auto detects code length

■ **Watch Dog**
- During timeout, outputs are system reset or interrupt.
- 32-bit down counter
- A variable time-out period of reset

■ **SD/MMC Controller**
- Two MMC/SD interfaces
- Fully compliant with MMCA v3.3
- Compliant with low-voltage support and 4 bits data of MMCA v4.0
- Compliant with SD/SDHC
- FAT16/FAT32 boot loader

■ **CCIR601/656**
- CCIR601/656 input for video capture

■ **TS Input/Output Interface**
- Supports TS serial mode
- 32 PID filters
- Maximum bit rate up to 100 Mbits

■ **Booting**
- Configurable booting media select
- SD/MMC/eMMC booting
- SPI-NAND booting
- NOR booting

■ **Suitable Product**
- Video Intercom System
- Access Control and Entrance System
- White Goods Display and Control
- Sports Equipment Display and Control
- Thermostat
- Smart Home Controller
- Display Controller

2. General Description

2.1 Introduction

The IT9850 series is high performance HD display and smart control SOC. (The IT9850 series include IT9852E . IT9854E and IT9856TE package.) It equips 2D Graphics Accelerator allowing for some special user interface designing, JPEG/H.264 HD decoding engine allowing users to have smooth experience while watching images and clips, audio engines allowing users to have joyful feeling while watching images and surely some other useful interfaces allowing users to have a more flexible using experience to be with their platform.

2.2 Multimedia Processor

2.2.1 High Performance 2D Graphics Accelerator

This engine supports bitblt, blending, rotation and scale function.

2.2.2 Powerful H.264 and JPEG Engine

The engines in the IT9850 offer users the ability to play those clips by video stream. The H.264 decoder engine can perform up to 1280x720p@30fps size clip decoding. Except for H.264 decoders, IT9850 has JPEG engine inside. The JPEG engine can perform up to 256M-pixel still JPEG decoding and perform up to 1280x720p@30fps motion JPEG clip decoding.

There is a video scaling engine for scaling up or down to the target display size.

2.2.3 Powerful Audio Solution

IT9850 embeds a 32-bit RISC CPU and a DSP engine. It can support MPEG-1 and MPEG-2 layer 2 audio decoder, MP3 decoder, HE-AAC decoder and FLAC decoder. IT9850 provides IIS as well. You can choose adopt another high performance IIS interface DAC freely for your consideration between performance and cost aspect.

2.2.4 High performance USB2.0 I/F

IT9850 supports a USB2.0 Host and a USB2.0 Device I/Fs. Users can have high speed data transfer experience through the USB2.0 I/F.

2.2.5 Flexible SPI-NAND/NOR flash controller and flash card I/Fs

IT9850 has various external cards, I/F, SPI-NAND flash I/F and NOR flash I/F. About external cards I/F, IT9850 builds in SD/MMC card controllers. If users want some other external cards I/F, IT9850 provides a USB host I/F allowing for an external card bus chip.

IT9850 provides SPI-NAND and NOR flash I/F. Users can choose SLC or MLC NAND Flash for both booting code and multimedia contents storage space. Besides SPI-NAND, NOR and SD are the other solutions for users to choose as a booting code storage space.

2.2.6 Display Interface

IT9850 supports various LCD I/Fs, such as RGB I/F, CPU I/F and CCIR601 I/F. To have better LCD supporting flexibility, IT9850 builds in digital T-con. With digital T-cons, users can save extra cost. Based on all these I/Fs, IT9850 can support resolution up to 1280x800 on true color mode.

Having the flexible display I/F, It will be easier to pick up the kind of LCM required for users' platform.

3. Block Diagram